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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/029,764	10/22/2001	Wen-Kun Yang	6033.P075	6437
23616	7590	02/24/2004	EXAMINER	
LAW OFFICES OF CLEMENT CHENG 17220 NEWHOPE STREET #127 FOUNTAIN VALLEY, CA 92708				WILLIAMS, ALEXANDER O
ART UNIT		PAPER NUMBER		
				2826

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/029,764	YANG ET AL.
	Examiner Alexander O Williams	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM
 THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on ____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) ____ is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) Claim(s) ____ is/are allowed.
- 6) Claim(s) ____ is/are rejected.
- 7) Claim(s) ____ is/are objected to.
- 8) Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on ____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. ____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. ____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: ____.

Art Unit: 2826

Serial Number: 10/029764 Attorney's Docket #: 0106-05169US
Filing Date: 10/22/01

Applicant: Yang et al.

Examiner: Alexander Williams

Applicant's Amendment, filed 12/5/03, has been acknowledged.

Claims 1 to 12 have been canceled.

The disclosure is objected to because of the following informalities: Divisional Patent Application information should be updated.

Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 13, 14 and 16 to 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Akagawa et al. (U.S. Patent # 5,960,308) in view of Masumoto et al. (U.S. Patent # 6,482,730 B1).

13. Akagawa et al. (figures 1 to 32) specifically figure 1 show a wafer level package **30** for producing chip size packages, comprising: a plurality of chips **32** on a surface of wafer (**inherit**); metal pads **36** formed on the surface of said wafer; photosensitive polymer layer **38** formed on the surface of said wafer and exposing said metal pads; a first conductive layer **40,41,43** formed on said metal pads within said photosensitive polymer layer; a circuit distribution pattern formed on the top of said photosensitive polymer layer and said first conductive layer; a protection layer **42** covered on said circuit distribution pattern, said photosensitive polymer layer and a portion of said circuit distribution pattern exposed; and conductive bumps **46** formed on said exposed circuit distribution pattern. Akagawa et al. fail to explicitly show a surface of the wafer having trenches running through, each said trench formed between said chips and a filling material filled in said trenches. However, this is shown in the process of making the device. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113.

Masumoto et al. is cited for showing a method of manufacturing a semiconductor device. Specifically, Masumoto et al. (figures 1 to 7) specifically figure 3(P) discloses show a surface of the wafer **32** having trenches **18** running through, each said trench formed between said chips and a filling material **19** filled in said trenches for the purpose of improving the sealing reliability of the semiconductor device.

14. The wafer level package according to claim 13, Akagawa et al.'s photo sensitive polymer comprises EPOXY

16. The wafer level package according to claim 13, Akagawa et al.'s filling material comprises EPOXY.

17. The wafer level package according to claim 13, Akagawa et al.'s protection layer comprises EPOXY.

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18. The wafer level package according to claim 13, Akagawa et al.'s conductive pattern diagram comprises copper.

19. The wafer level package according to claim 13, Akagawa et al.'s conductive bump comprises solder.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Masumoto et al.'s trenches in the wafer-level package to modify Akagawa et al.'s semiconductor device for the purpose of improving the sealing reliability of the semiconductor device.

Claims 13, 14 and 16 to 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Chakravorty (U.S. Patent # 6,181,569 B1) in view of Masumoto et al. (U.S. Patent # 6,482,730 B1).

13. Chakravorty (figures 3 to 9f) specifically figure 6 show a wafer level package **30** for producing chip size packages, comprising: a plurality of chips **301** on a surface of wafer (**inherit**); metal pads **303** formed on the surface of said wafer; photosensitive polymer layer **305** formed on the surface of said wafer and exposing said metal pads; a first conductive layer **397,310** formed on said metal pads within said photosensitive polymer layer; a circuit distribution pattern formed on the top of said photosensitive polymer layer and said first conductive layer; a protection layer **308** covered on said circuit distribution pattern, said photosensitive polymer layer and a portion of said circuit distribution pattern exposed; and conductive bumps **311** formed on said exposed circuit distribution pattern. Akagawa et al. fail to explicitly show a surface of the wafer having trenches running through, each said trench formed between said chips and a filling material filled in said trenches. . However, this is shown in the process of making the device. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear. As to the grounds of rejection under section 103, see MPEP § 2113.

14. The wafer level package according to claim 13, Chakravorty's photosensitive polymer comprises EPOXY
16. The wafer level package according to claim 13, Chakravorty's filling material comprises EPOXY.
17. The wafer level package according to claim 13, wherein said protection layer comprises EPOXY.
18. The wafer level package according to claim 13, Chakravorty's conductive pattern diagram comprises copper.
19. The wafer level package according to claim 13, Chakravorty's conductive bump comprises solder.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Chakravorty's trenches in the wafer-level package to modify Akagawa et al.'s semiconductor device for the purpose of improving the sealing reliability of the semiconductor device.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Chakravorty (U.S. Patent # 6,181,569 B1) in view of Masumoto et al. (U.S. Patent # 6,482,730 B1) and further in view of Ishida (U.S. Patent # 5,686,702).

Chakravorty and Masumoto et al. show the features of the claimed invention as detailed above, but fail to explicitly show the said photosensitive polymer comprises photo PI.

Ishida is cited for showing a polyimide multilayer wiring substrate. Specifically, Ishida (figure 1) discloses where photosensitive polymer comprises photo PI for the purpose of preventing the occurrence of cracks and fractures in the polyimide resins.

Therefore, it would have been obvious to one of ordinary skill in the art to use Ishida's polymer to modify Chakravorty's polymer for the purpose of preventing the occurrence of cracks and fractures in the polyimide resins.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Akagawa et al. (U.S. Patent # 5,960,308) in view of Masumoto et al. (U.S. Patent # 6,482,730 B1) and further in view of Ishida (U.S. Patent # 5,686,702).

Akagawa et al. and Masumoto et al. show the features of the claimed invention as detailed above, but fail to explicitly show the said photo sensitive polymer comprises photo PI.

Ishida is cited for showing a polyimide multilayer wiring substrate. Specifically, Ishida (figure 1) discloses where photosensitive polymer comprises photo PI for the purpose of preventing the occurrence of cracks and fractures in the polyimide resins.

Therefore, it would have been obvious to one of ordinary skill in the art to use Ishida's polymer to modify Masumoto et al./Akagawa et al.'s polymer for the purpose of preventing the occurrence of cracks and fractures in the polyimide resins.

Response

Applicant's arguments filed 12/5/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,620,618,787,737,738,778,772,734, 700,701,758,759	9/21/03 2/21/04
Other Documentation: foreign patents and literature in 257/686,685,723,777,620,618,787,737,738,778,772,734, 700,701,758,759	9/21/03 2/21/04
Electronic data base(s): U.S. Patents EAST	9/21/03 2/21/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (703) 308 4863. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308 6601. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
2/22/04



Alexander Williams
Primary Examiner

ALL DRAWINGS	O.G. FIG.
BY	CLASS SUBCLAS.
DRAFTSMAN	

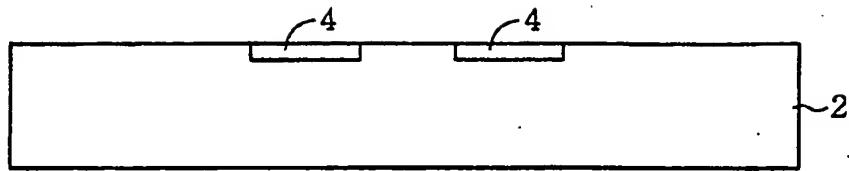


FIG. 1

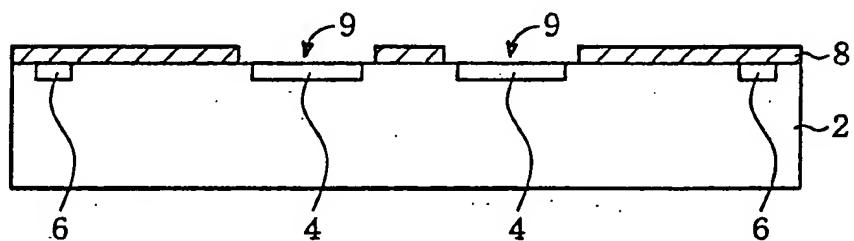


FIG. 2

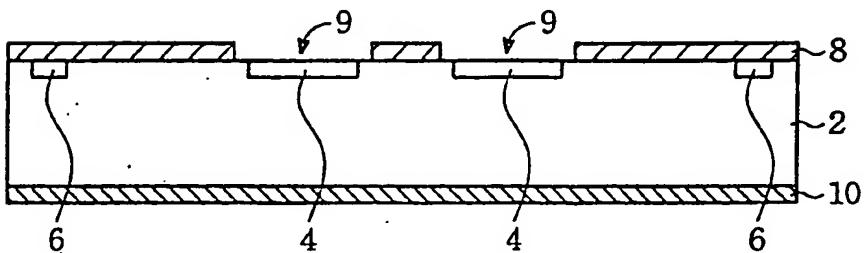


FIG. 3

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

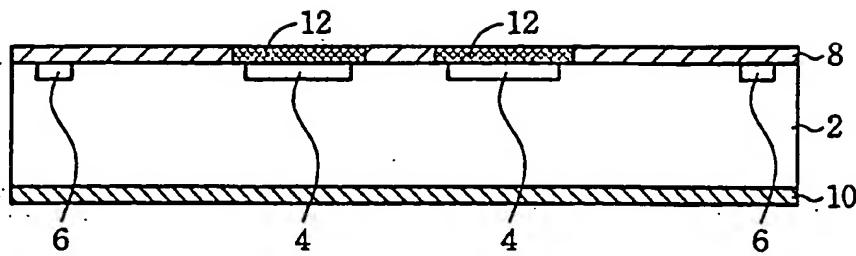


FIG. 4

10026754-1.DOCX

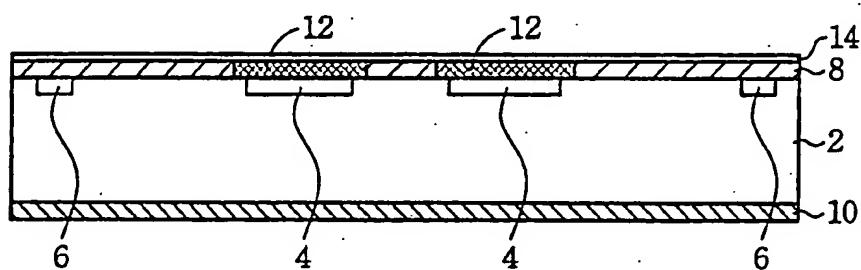


FIG. 5

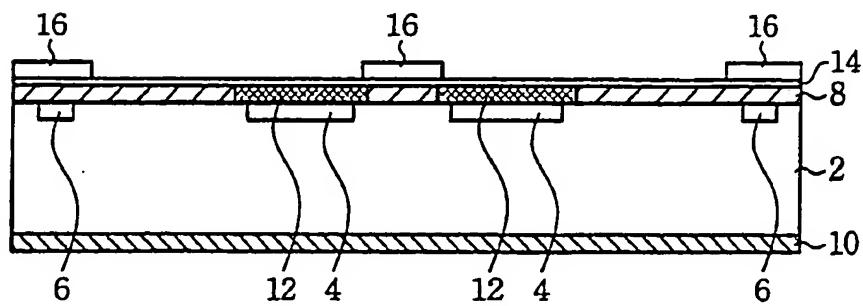


FIG. 6

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

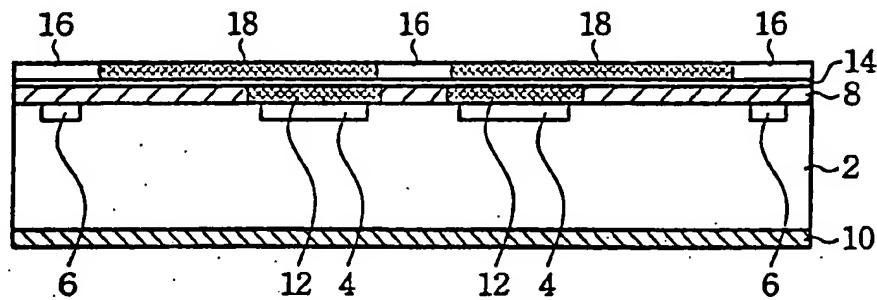


FIG. 7

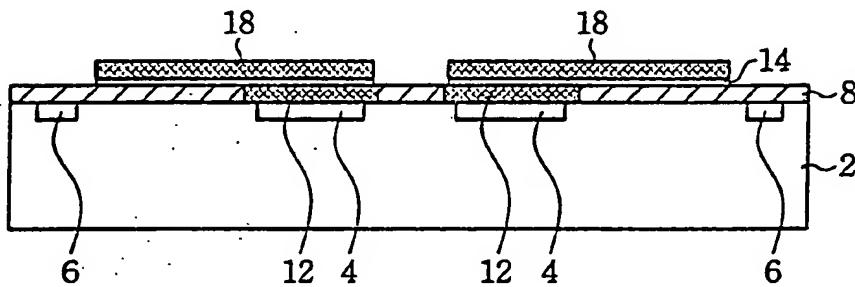


FIG. 8

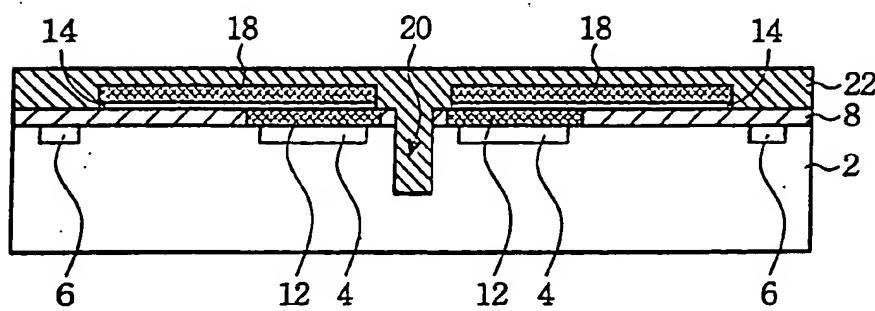
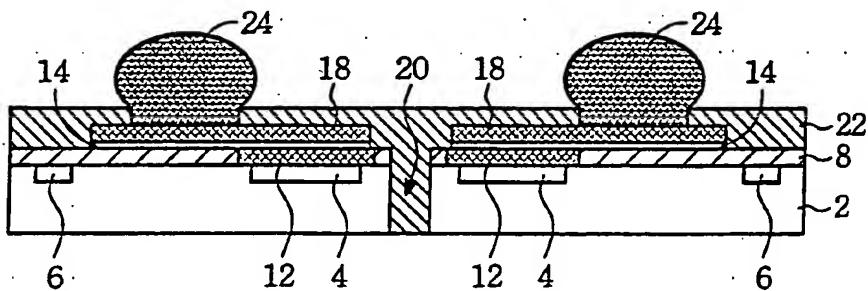
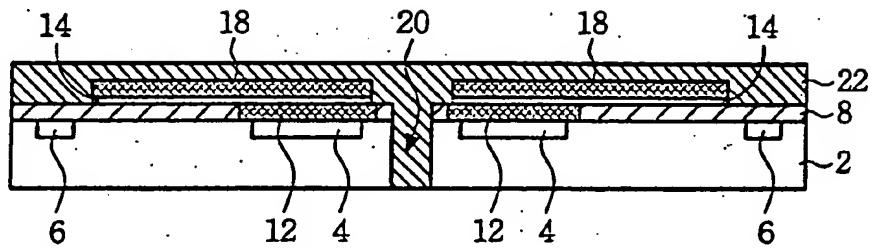


FIG. 9

FOR PAPER "THE 262000"

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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APPROVED	D.G. FIG.
BY	CLASS SUBCLASS
GRAFTSMAN	

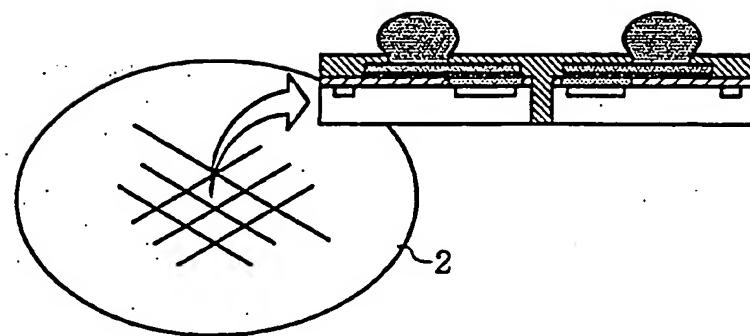


FIG. 12

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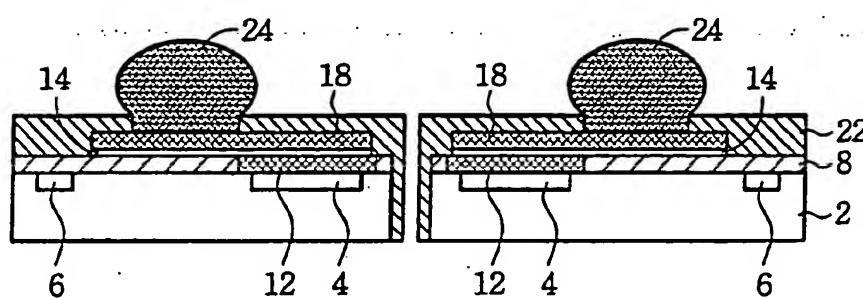


FIG. 13